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TECHNICAL DATA

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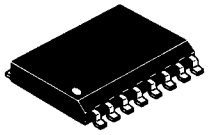
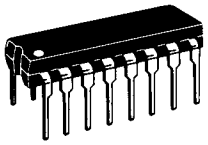
MCCS1850



DW SUFFIX
SOG
CASE 751G



P SUFFIX
PLASTIC
CASE 648

Ordering Information

MCCS1850DW	SOG
MCCS1850P	PDIP

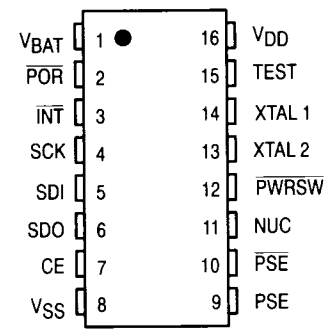
Advance Information

Serial Real-Time Clock

The MCCS1850 is a Real-Time Clock (RTC) used for keeping time in computer systems during both power-up and power-down modes. In respect to serial interfacing with a microprocessor unit (MPU), this device is similar to the MC68HC68T1 Real Time Clock. However, internal operation of the MCCS1850 is much more simplified and additional analog features for power cycling have been incorporated. Some other features include:

- 32-bit counter (plus 32-bit read latch) incremented once per second
- Alarm implemented with 32-bit latch and 32-bit comparator
- 64 bytes of RAM
- Operational to 2.2 volts (from battery)
- Power-on reset detects first time up
- Power on/off switch and power supply enable interface
- Power supply auto-restart (for file server applications)
- Serial interface operation
- Configured as 64 bytes of RAM and 10 bytes of registers

PIN ASSIGNMENT



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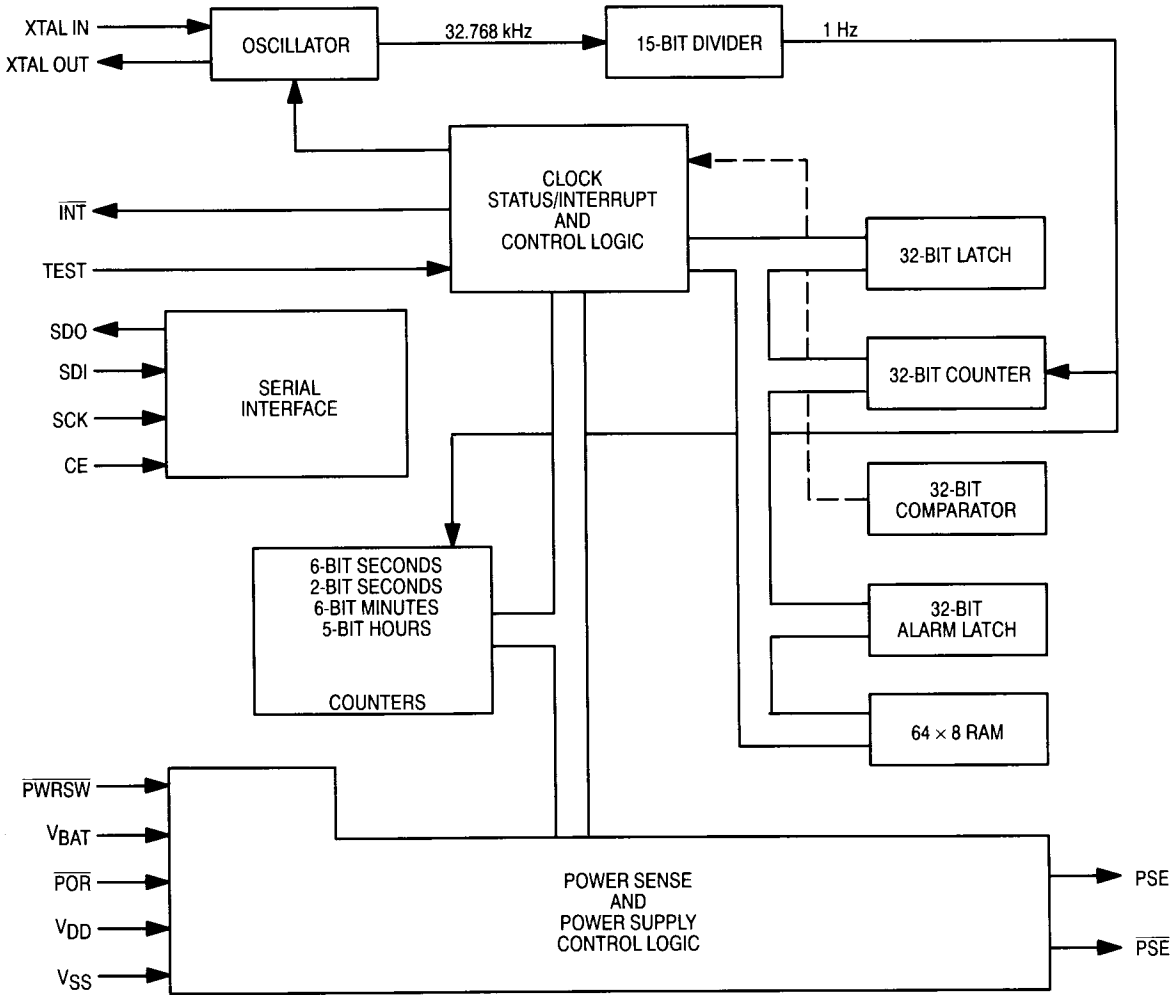
This document contains information on a new product. Specifications and information herein are subject to change without notice.

CONTENTS

FUNCTIONAL BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Min	Max	Unit
Supply Voltages	V_{DD}	− 0.5	6.5	V
Battery Power Supply	V_{BAT}	− 0.5	—	V
All Input Voltages	V_{in}	− 0.5	V_{DD} + 0.5	V
All Output Voltages	V_{out}	− 0.5	V_{DD} + 0.5	V
All Input Current	I_{in}	± 20	—	mA
All Output Current	I_{out}	± 20	—	mA
Supply Current	I_{DD}, I_{SS}	—	± 50	mA
Power Dissipation (See Note 2)	P_D	—	500	mW
Operating Temperature Range	T_A	0	70	°C
Storage Temperature	T_{stg}	− 65	150	°C
Lead Temperature (8 Second Soldering)	T_L	—	260	°C

NOTES:
1. Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics tables or pin descriptions sections.
2. Power dissipation temperature de-rating – 12 mW/°C from 65°C to 85°C.

1.2 DC CHARACTERISTICS — Standby (T_A = 0°C to 70°C, V_{BAT} = 2.2 V to 3.5 V, V_{DD} = 0 V, unless otherwise noted. Voltages referenced to V_{SS})

Characteristic	Test Condition	Symbol	Min	Max	Unit
Standby Operating Current	V_{in} = 0 V I_{out} = 0 µA	I_{BAT}	—	20	µA

1.3 DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{BAT} = 2.2 V to 3.5 V, V_{DD} = 4.5 to 5.5 V, unless otherwise noted. Voltages reference to V_{SS})

Characteristic	Test Condition	Symbol	Min	Max	Unit
Input Low Voltage All inputs except XTAL1 and PWRSWB		V_{IL}	—	0.9	V
Input High Voltage All inputs except XTAL1 and PWRSWB		V_{IH}	2.4	—	V
Output Low Voltage	I_{out} = 20 µA I_{out} = ± 1.6 mA	V_{OL}	— —	0.8 0.8	V
Output High Voltage	I_{out} = 20 µA I_{out} = ± 1.6 mA	V_{OH}	2.4 2.4	— —	V
Input Current — XTAL1 Other Inputs (See Note)		I_{in}	± 1	± 10	µA
Output High Current All outputs except XTAL2 and PSE PSE		I_{OH}	 — —	 − 1.6 − 10	mA

NOTE: Serial interface pins have active pulldowns. Refer to **Serial Interface** for further information.

(Continued)

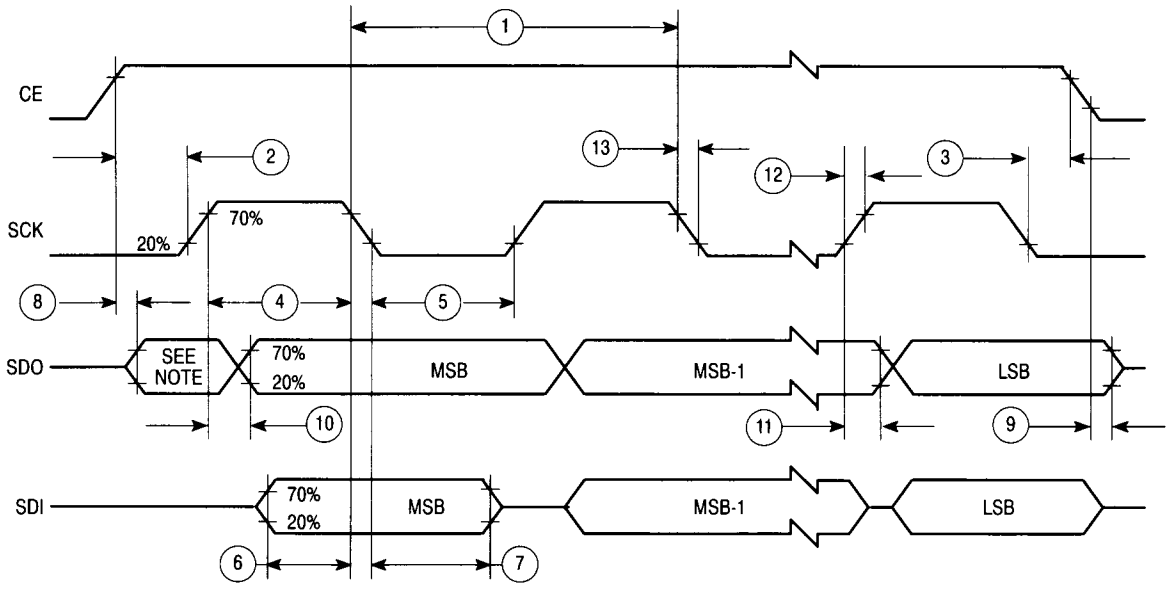
1.3 DC CHARACTERISTICS (Continued)

Characteristic	Test Condition	Symbol	Min	Max	Unit
Output Low Current All outputs except XTAL2 and PSE PSE		I_{OL}	 — —	 1.6 10	mA
Input Capacitance — XTAL1		C_{in}	2.5	20	pF
High-Impedance Output Capacitance		C_{out}	—	20	pF
High-Impedance Output Current		I_{OZ}	—	± 10	µA
Operating Current	V_{in} = 0 or V_{DD}, I_{out} = 0 µA, V_{BAT} = 3 V	I_{DD}	2	10	mA

NOTE: Serial interface pins have active pulldowns. Refer to **Serial Interface** for further information.

1.4 AC CHARACTERISTICS (V_{DD} = 5.0 V ± 5%, T_A = 0°C to 70°C, C_L = 50 pF, unless otherwise noted)

Num.	Characteristic		Symbol	Min	Max	Unit
1	Cycle Time		t_{cyc}	475	—	ns
2	Chip Enable Lead Time		t_{lead}	150	—	ns
3	Chip Enable Lag Time		t_{lag}	150	—	ns
4	CLock (SCK) High Time		t_{wh}	190	—	ns
5	Clock (SCK) Low Time		t_{wl}	190	—	ns
6	Data Setup Time		t_{su}	100	—	ns
7	Data Hold Time (Input)		t_{thi}	50	—	ns
8	Access Time (Data active to high-impedance)		t_{acc}	0	120	ns
9	Disable Time (Data active to high-impedance)		t_{dis}	—	100	ns
10	Data Valid (After clock edge)		t_{dv}	—	100	ns
11	Data Hold Time (Output)		t_d	0	—	ns
12	Rise Time (20% to 70% V_{DD}, C_L = 200 pF)	Output — SDO Input — SDI Inputs — CE, SCK	t_{ro} t_{rdin} t_r	— — —	100 10 1	ns µs ms
13	Fall Time (70% ot 20% V_{DD}, C_L = 200 pF)	Output — SDO Input — SDI Inputs — CE, SCK	t_{fo} t_{fdin} t_f	— — —	100 10 1	ns µs ms



NOTE: Not defined but normally LSB of previously transmitted character.

MSB = Most Significant Bit
LSB = Least SIgnificant Bit

Figure 1. Single Byte Timing

2.0 PIN DESCRIPTIONS

V_{BAT} — BATTERY VOLTAGE (Pin 1)

This pin is connected to the battery through a current limiting resistor. This pin supplies power to the internal power bus when the V_{DD} pin voltage is less than the voltage at the V_{BAT} pin. An internal camparator senses this condition. During the standby mode of operation, for the conditions described above, V_{BAT} supplies power to the oscillator, the 15-bit ripple counter, the 32-bit seconds counter, the alarm circuitry, and all RAM. To minimize standby I_{DD}, all other devices are not activated during the standby mode.

$\overline{POR}$ — Power-On Reset (Input/Output, Pin 2)

This active low pin is used to generate a power-on reset. An external capacitor tied to this pin determines the power-on reset timing when voltage is applied to V_{BAT}. Anytime a $\overline{POR}$ is generated, the First Time Up bit (Register $30, bit 4 — FTU) is set.

$\overline{INT}$ — INTERRUPT (Output, Pin 3)

This active-low output is driven from a single N-channel transistor and must be tied to an external pullup resistor. The pin is driven low when the Interrupt True (IT) bit of the Status/Interrupt register (register $30, bit 3) is set. See Interrupts for a description of sources of interrupts.

SCK — SERIAL CLOCK (Input, Pin 4)

This serial clock input is used to shift data into and out of the on-chip interface logic. The SCK pin has an active internal pull-down (100K) that is activated when $V_{DD} < (V_{BAT} \times 1.25)$. The state of the SCK pin is normally low.

SDI/SDO — SERIAL DATA IN/SERIAL DATA OUT (Input and Output, Pins 5 and 6)

Data is shifted into the SDI pin and out of the SDO pin on the rising edge of SCK and latched on the falling edge of SCK internally. This is equivalent to the MC68HC68T1 serial interface timing with clock polarity equal to zero. The SCK pin is not operational when the chip enable (CE) pin is in the inactive state. The SDO pin goes into a high-impedance state when the CE pin is negated or when the access is a write operation. The SDI pin has an active internal pull-down (100K) that is activated when $V_{DD} < (V_{BAT} \times 1.25)$.

CE — CHIP ENABLE (Input, Pin 7)

When high, the chip enable input activates the interface logic, otherwise the logic is in a reset state. The CE pin has an active internal pull-down (100K) that is activated when $V_{DD} < V_{BAT} \times 1.25$. Additional internal circuitry disables the state of the CE pin until $V_{DD} > (V_{BAT} \times 1.25)$.

PSE — POWER SUPPLY ENABLE (Output, Pin 9)

When active high, this output enables the system power supply. PSE is capable of sourcing 10 mA current with an output high voltage of $V_{DD} - 0.6$ volt. Power for this output pin is supplied by the internal power bus and V_{SS}. PSE may be negated by writing a one to the Power-Down bit in the Clock Control register ($31). PSE may only be asserted when $V_{DD} > V_{BAT}$. This limitation is imposed to allow the power supply to respond to a power-up request by the RTC. V_{DD} is not connected to the PSE pin internally in the MCCS1850 until $V_{DD} > V_{BAT}$.

$\overline{PSE}$ — POWER SUPPLY ENABLE (Output, Pin 10)

This open-drain output is used for driving external transistor circuitry that is used for transitions to and from the battery supply voltage.

The pin is the complement of the $\overline{PSE}$ pin. It is powered from the internally switched power bus. $\overline{PSE}$ is negated when $V_{DD} > (1.25 \times V_{BAT})$. For a functional description, refer to **Power Up** and **Power Down**.

NUC — NO USER CONNECTION (Output, Pin 11)

This pin outputs the buffered 32-kHz signal in test mode when bit 7 of Test Register 1 is set or when DV2, DV1, DV0 are set to '001' in Test Register 2. Otherwise this pin is three-stated.

$\overline{PWRSW}$ — POWER SWITCH (Input, Pin 12)

This input is connected to the power on/off switch. The other side of the switch is connected to ground. $\overline{PWRSW}$ has a Schmitt-trigger input and an internal pullup resistor (100K).

XTAL1, XTAL2 — CRYSTAL INPUT/OUTPUT (Input/Output, Pins 13 and 14)

For crystal operation, the two pins are connected to a 32.768 kHz crystal. The optimum load capacitance for the crystal is designed to be 6 pF. If an external clock is used, connect the external clock to XTAL1 and leave XTAL2 unconnected. The external clock must swing from 0% to 50% V_{DD} with a DC offset of 25% V_{DD}.

TEST — TEST MODE (Pin 15)

When this pin is taken high, the test mode is entered. The status of the pin is reported at bit 5 in the Clock Status and Interrupt register ($30). This pin has an internal 20K pull-down resistor. This pin should be tied to V_{SS} during normal operation. This pin should not change state during normal operation.

V_{DD} — POWER (Input, Pin 16)

+ 5 volts supply input. V_{DD} ranges from + 4.5 to + 5.5 V with respect to V_{SS}.

V_{SS} — POWER (Pin 8)

This pin is connected to system ground.

3.0 ADDRESS MAP

The address map is divided into RAM, real-time clock alarm and counter, status and control registers, test registers, and test mode counter. Address locations are shown in Table 1.

Address (Hex)	Function	Description
$00–$1F	RAM	32 Bytes
$20–$27	Registers	Clock and Alarm
$30–$31	Registers	Status and Control
$3E–$3F	Registers	Test Mode
$40–$4F	Counters	Test Mode Only
$40–$5F	RAM	32 Bytes
$60–$7F		Reserved

The test mode is entered by taking the test pin high. In the test mode, the address locations $40–$4F are reserved for breaking the large divider chains and counters into byte addressable locations. The locations $60–$7F are reserved for future expansion. A read or write of the Test registers ($3E–$3F) while not in the test mode is undefined.

TEST MODE ADDRESS MAP OF COUNTER BREAKUP

$40 Kick-Start Counter LSB (Bits 0–7)
$41 Kick-Start Counter Middle Byte Segment (Bits 8–15)
$42 Kick-Start Counter 2 MSB (Bits 16, 17)
$43 Prescale Counter LSB (Bits 0–7)
$44 Prescale Counter 7 MSB (Bits 8–14)
$4F Test Mode Counter Increment
(A write to $4F will increment each segment of the above 2 registers and the clock counter.)

4.0 REGISTER DESCRIPTIONS

4.1 CLOCK STATUS/INTERRUPT AND CONTROL LOGIC

The Clock Chip registers consist of a 4-byte (32-bit) binary counter plus latch ($20–$23), a 4-byte alarm latch ($24–$27), the Status/Interrupt register ($30) and the Control register ($31). The 32-bit counter is incremented once per second. The 32-bit latch associated with the 32-bit counter is loaded from the 32-bit counter when a read of the most significant byte, MSB, ($20) is detected. Data from the counter is not loaded into the latch unless a read of the MSB is detected. This is meant to conserve power during battery backup mode of operation.

4.2 CLOCK AND ALARM DATA REGISTERS — 8 BITS — READ/WRITE — $20–$27

BIT	7	6	5	4	3	2	1	0
$20	Counter/Latch Byte 0							MSB
$21	Counter/Latch Byte 1							
$22	Counter/Latch Byte 2							
$23	Counter/Latch Byte 3							LSB
$24	Alarm Latch Byte 0							MSB
$25	Alarm Latch Byte 1							
$26	Alarm Latch Byte 2							
$27	Alarm Latch Byte 3							LSB

4.3 CLOCK STATUS/INTERRUPT REGISTER — 8 BITS — READ ONLY — $30

BIT	7	6	5	4	3	2	1	0
$30	1	0	TM	FTU	IT	LB	AI	RPD

Bit	Function
7	This bit is always 1. Software can check this bit to determine which device is in place. This bit is always low in the MC68HC68T1.
6	This bit is not used and is always 0.
5	TM — TEST MODE This bit reports the status of the test mode pin. Note that the test mode pin does not cause an interrupt to be generated.
4	FTU — FIRST TIME UP FTU is set to a 1 by Power-On Reset and causes the Interrupt True bit (bit 3) to be set.
3	IT — INTERRUPT TRUE This bit is set if one of the interrupts is valid. When set, IT causes the $\overline{INT}$ pin to be asserted to a logic low level. When the function causing the interrupt is serviced, IT is negated
2	LB — LOW BATTERY Whenever the voltage on the V_{BAT} pin < $0.44 \times V_{DD}$, and bit LBE (bit 1, register $31) is enabled LB is set. When set, LB sets the IT bit (bit 3) and an interrupt is generated.
1	AI — ALARM An active high value indicates that the current value in the alarm latch and the counter have matched and that AE (bit 4, register $31) was enabled while $V_{DD} > V_{BAT} \times 1.25$. When set, AI causes the IT bit (bit 3) is set and an interrupt is generated.
0	RPD — REQUEST TO POWER DOWN This is a status bit which is set when the device is operating on V_{DD} (V_{DD} > 4.5 V) and the $\overline{PWRSW}$ is momentarily grounded. When set, the IT bit (bit 3) is set and an interrupt is generated.

All bits in the Status register are reset to 0 by a Power-On Reset with the exception of FTU (bit 4) which is set to '1'.

4.4 CLOCK CONTROL REGISTER — 8 BITS — READ/WRITE — $31

BIT	7	6	5	4	3	2	1	0
$31 Write	STR/$\overline{\text{STP}}$	PD	AR	AE	AC	FTUC	LBE	RPDC
$31 Read	STR/$\overline{\text{STP}}$	PD	AR	AE	0	0	LBE	0

Bit	Function
7	STR/$\overline{\text{STP}}$ — START/$\overline{\text{STOP}}$ This bit is used to enable and disable counting of the 32-bit counter. When start is 1, the 32-kHz oscillator and 2^{15} divider continues to count. When a write of a 1 is detected the 2^{15} divider is reset to 0, effectively setting the count to a known state.
6	PD — POWER DOWN When set to 1, PD initiates a power down by setting PSE pin to a logic 0.
5	AR — AUTO RESTART When set to 1, AR enables the auto restart sequence. See **Auto Reset** for more information.
4	AE — ALARM ENABLE When set to 1, AE enables the output of the alarm comparator.
3	AC — ALARM CLEAR Writing a 1 to AC will clear bit 1 (alarm interrupt) of the Clock Status/Interrupt register ($30). This bit always reads as 0.
2	FTUC — FIRST TIME UP CLEAR Writing a 1 to FTUC will clear bit 4 (first time up) of the Clock Status/Interrupt register ($30). This bit always reads as 0.
1	LBE — LOW BATTERY ENABLE Setting LBE to a 1 will enable bit 3 (interrupt true) of the Clock Status/Interrupt register to be set when the condition of bit 2 (low battery) of the Clock Status/Interrupt register ($30) is true.
0	RPDC — REQUEST TO POWER DOWN CLEAR Writing a 1 to RPDC will clear bit 0 (request to power down) of the Clock Status/Interrupt register ($30). This bit always reads as 0.

All bits in the control register are reset by a power-on reset. Bits 6, 3, 2, and 0 are not latched, they would subsequently read a zero after a 1 is written to these locations.

4.5 INTERRUPTS

There are four different interrupt sources:

1. AI (Alarm Interrupt, register $30, bit 1) with AE (Alarm Enable, register $31, bit 4) and AC (Alarm Clear, register $31, bit 3) while in power up ($V_{DD} > V_{BAT} \times 1.25$) mode.
2. LB (Low Battery, register $30, bit 3) with LBE (Low Battery Enable, register #31, bit 1).
3. FTU (First Time Up, register $30, bit 4) with FTUC (First Time Up Clear, register $31, bit 2).
4. RPD (Request to Power Down, register $30, bit 0) with RPDC (Request to Power Down Clear, register $30, bit 0).

The Alarm Interrupt is generated when a match between the real-time clock counter ($20–$23) and the alarm latch bytes ($24–$27) occurs provided that the alarm is enabled by AE when in power-up mode.

The Low Battery Interrupt is generated when the battery voltage at the VBAT pin drops below $0.44 \times V_{DD}$ volts and the Low Battery interrupt is enabled.

The First Time Up interrupt is meant to signal that the contents of the RAM or clock are not valid. First time up has no enable bit but does include a clear bit.

The function of the Request to Power Down (and clear) is as follows:

— When operating on power from the V_{BAT} pin (battery) and the $\overline{PWRSW}$ momentarily grounded, the PSE and $\overline{PSE}$ pins will be asserted without setting the RPD bit of the Clock Status Register ($30, Bit 0).

— When operating on the V_{DD} pin (supply) and $\overline{PSRSW}$ is momentarily grounded, the RPD bit is set and causes an interrupt.

— The power-down sequence is to clear RPD by writing a 1 to the RPDC (register $31, bit 0) bit and then writing a 1 to the PD (register $31, bit 6) bit. A write to the PD bit will cause the PSE pin to be negated (go low).

5.0 POWER CONTROL LOGIC

The MCCS1850 contains a power supply interface which monitors the power on/off switch, signals power switch state and generates power supply enable signals. The power switch is monitored by $\overline{PWRSW}$. The PSE and $\overline{PSE}$ pins supply current for driving external loads for power supply cycling.

5. 1 POWER UP

In the standby mode, (i.e., V_{DD} = 0 V), the PSE pin will be driven high and the $\overline{PSE}$ pin will be driven low when any one of the following conditions exists:

1. The power on/off switch is momentarily closed (path to ground).
2. The Auto Restart bit (register $31, bit 5) is high.
3. The 32-bit alarm comparator is true with AE set and $V_{DD} < V_{BAT}$ (i.e., in standby mode).

Event #1 has the highest priority, followed by #2, then #3. However, there are two special cases: 1) with event #2, if $\overline{PWRSW}$ is closed and AR = 1, then PSE and $\overline{PSE}$ are asserted immediately. 2) When an alarm match occurs with AR = 1, timing for the AR function is used for asserting PSE/$\overline{PSE}$ and the alarm match is not reported in the AI status Bit.

The $\overline{PSE}$ pin will be driven low for up to 4 seconds. If the power supply asserts V_{DD} within 4 seconds, the low level on the $\overline{PSE}$ pin will be maintained until $V_{DD} = 1.25 \times V_{BAT}$. If the auto restart bit is high, the clock chip will retry $\overline{PSE}$ for 4 seconds once every 64 seconds up to 36 hours ($64 \times 64 \times 32$ = 131,072 seconds ± 36.41 hours) or until the power supply asserts V_{DD}. For example, in a typical application, the power supply would normally respond for the first two cases. The Auto Restart feature allows retries if the power supply does not respond on the first try.

The PSE pin is powered by an internally switched power bus while the $\overline{PSE}$ pin is an open-drain output. The internal power bus switches from V_{DD} to V_{BAT} and vice versa during power cycling. An internal comparator compares the V_{DD} supply with the battery voltage (normally 3.0 V). $\overline{PSE}$ is negated when $V_{DD} > (1.25 \times V_{BAT})$, while PSE stays asserted until one of the conditions necessary for power down are met. See Figure 2.

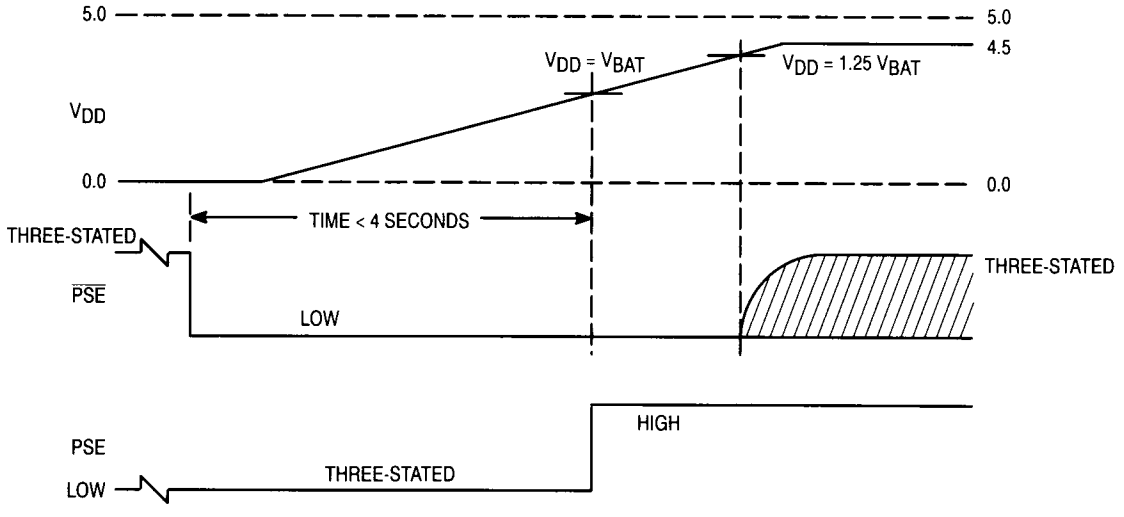


Figure 2. Power-Up Sequence

5. 2 POWER DOWN

If the MCCS1850 is operational (i.e., $V_{DD} > V_{BAT} \times 1.25$), the PSE pin will be reset low by writing a 1 to the Power Down bit (PD — bit 6 of the Clock Control register, $31). The state of the $\overline{PSE}$ pin remains unchanged.

Request to Power Down (RPD) and Request to Power Down Clear (RPDC) may also be used in conjunction with the PD bit. Refer to Interrupts for a description of these operations.

During a power cycle, V_{DD} is recognized to be greater than $1.25 \times V_{BAT}$ (3.75 V @ V_{BAT} = 3.0) serial interface is enabled. When voltages are less than $1.25 \times V_{BAT}$ (3.75 V @ V_{BAT} = 3.0), the serial interface is disabled.

5.3 POWER-ON RESET

Power-On Reset (POR) has two functions:

1. In the user mode, resets all the bits in the Clock Control register. POR sets the First Time up (FTU) bit in the Status/Interrupt register ($30), and sets RAM to $FF.
2. In the test mode, used to reset internal states of logic.

POR is generated by an application of power to the V_{BAT} pin. POR timing produces a signal delay of 10 µs typically for V_{BAT} rise time of 20 ns. When the rise time of V_{BAT} approaches 10 ms a delay period of 0.1 to 1,000 µs can be expected. Refer to **Test Registers** for an operational description of the generation of POR.

5.4 COMPARATORS

Three comparators are used within the MCCS1850. Two of the three comparators are used to control power cycling to and from the power supply and battery. A third comparator informs the user of a low battery voltage indicating that battery backed up data may be invalid.

1. CVDDUP — The V_{DD} voltage is compared against the V_{BAT} voltage. CVDDUP is '1' if $V_{DD} > V_{BAT} \times 1.25$.
2. CVDDON — The V_{DD} voltage is compared against the V_{BAT} voltage. The comparator switch point occurs when V_{DD} pin voltage is equal to V_{BAT} pin voltage. This transition is smooth with no internal power glitching. CVDDON is '1' if $V_{DD} > V_{BAT}$.
3. CLOWBAT — The V_{BAT} pin voltage is compared against $V_{BAT} \times 2.2$. The status of this comparator is reported by the Low Battery Status bit in the Clock Status/Interrupt register ($30). CLOWBAT is '1' if $V_{DD} > V_{BAT} \times 2.2$

The status of these comparators may be read in the test mode via bits 5, 4, and 3 of register $3E.

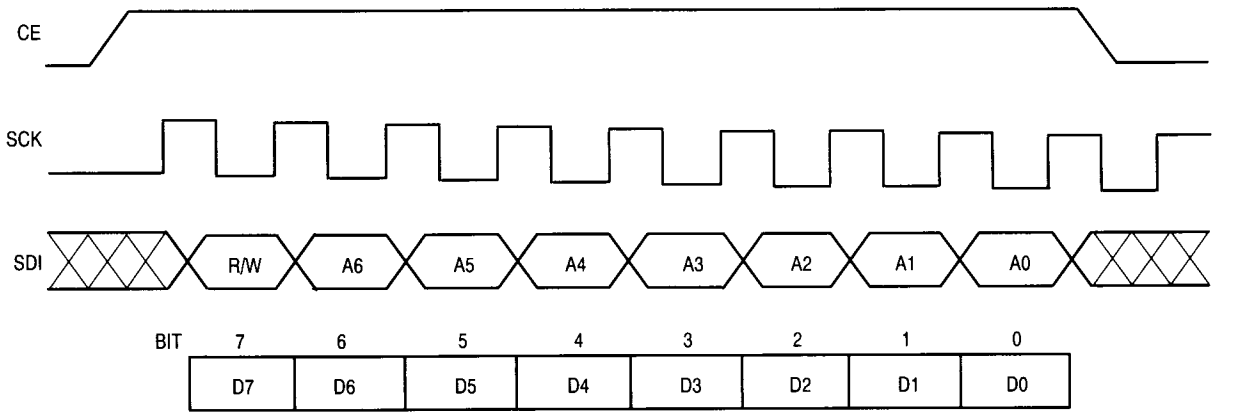
6.0 SERIAL INTERFACE

The serial peripheral interface (SPI) utilized by the MCCS1850 is a serial synchronous bus for address and data transfers. Four pins are utilized for transferring addresses and data: Serial Clock (SCK), Serial Data In (SDI), Serial Data Out (SDO), and Chip Enable (CE). Data is shifted out of the SDO pin on the rising edge of SCK and latched at the SDI pin on the falling edge of SCK. See Figure 3.

The address/control and data bytes are shifted Most Significant Bit (MSB) first, into the SDI and out of the SDO pin. Any transfer of data requires the address/control byte to specify a write or read operation and to select an address location. This byte is followed by one or more bytes of data. Multiple data bytes may be sent as long as CE is asserted. Internally an address counter increments after each data byte is received. The address counter has a maximum count value of $7F and rolls over to zero.

After CE is asserted, the first byte entered is always the Address/Control byte. Data shifted out of the SDO pin during an address byte transfer should be ignored. To transmit a new address the CE pin must be negated and then re-asserted.

Refer to Figures 4 and 5 for examples of single-byte and multiple-byte data transfers.



NOTES:
Bit 7 — $\overline{R}$/W — $\overline{Read}$/Write
High — Initiates one or more write cycles
Low — Initiates one of more read cycles
Bit 6 — A6–A0
Selects a 7-bit address of RAM or specifies a clock register.

Figure 3. Address/Control Byte

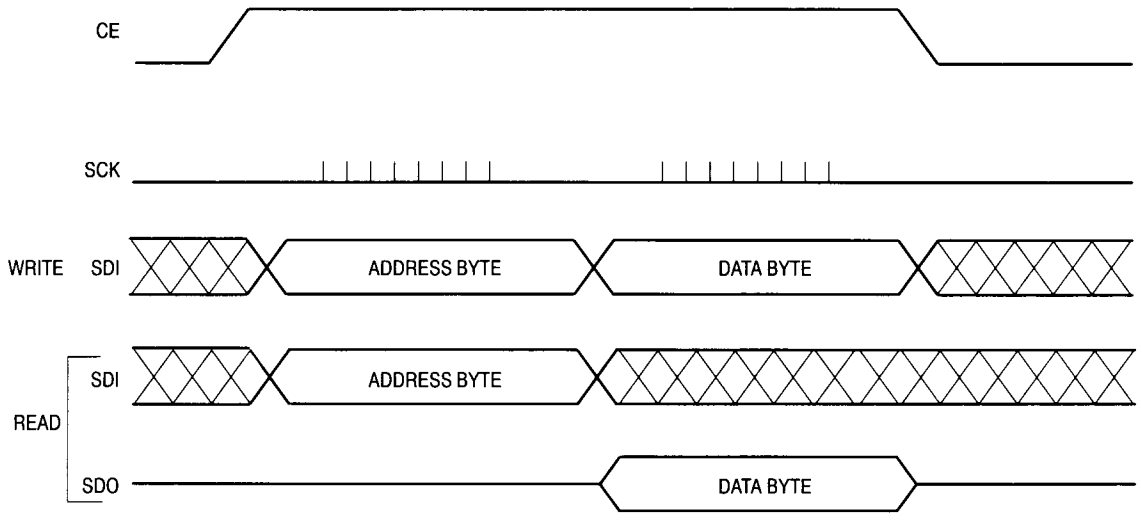


Figure 4. Single-Byte Transfer

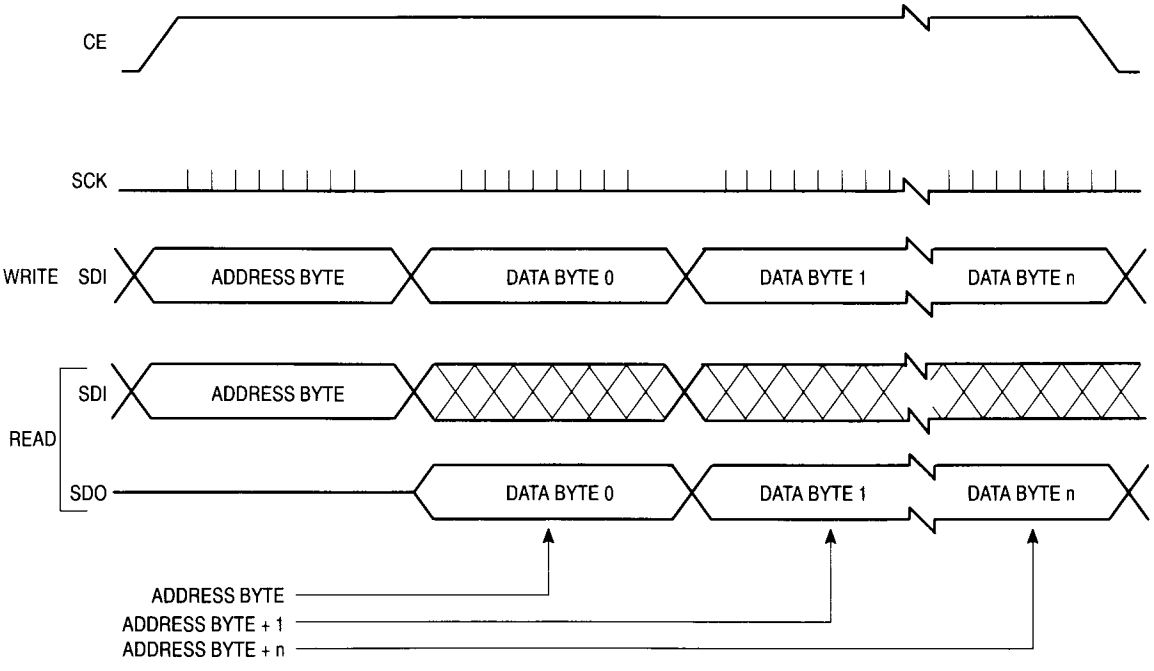


Figure 5. Multiple-Byte Transfer

7.0 OSCILLATOR

The oscillator consists of a single-stage inverter with additional circuitry for enabling/disabling operation and tuning bits that allows adjustment of the operating frequency.

The oscillator and the first two divider stages of the 15-bit counter are operated at reduced voltage swings to minimize standby current consumption. Level shifting occurs after the second divider stage (8 kHz).

Crystal Specifications

The MCCS1850 crystal specifications include:

Mode:	Parallel Fundamental Resonant Mode
Load Capacitance:	6 pF
Series Resistance:	> 30K ohms
Tolerance:	20 ppm

8.0 AUTO-RESTART COUNTERS

The counters are used to implement the Auto Restart feature as described in **Power Up**. There are four different counters:

1. A 2-bit counter clocked by a 1-Hz input clock generates a 4 second window for the Auto Restart interval in which the PSE pin may be driven high.
2. A 6-bit counter clocked by a 1-Hz input clock to generate 64 seconds.
3. A 6-bit counter clocked by the output of the seconds counter to generate minutes.
4. A 5-bit counter clocked by the output of the minutes counter to generate hours.

The basic time interval function can be described by: [1 Hz][$2^6 \times 2^6 \times 2^5$] = 131,072 seconds (approximately 36.41 hours). The counters are enabled when the Auto Restart bit (bit 5, register $31) is set and the Standby Mode is entered . The counters are reset when V_{DD} is greater than $V_{BAT} \times 1.25$ volts.

9.0 COUNTER AND ALARM FUNCTIONS

The 32-bit counter is a binary counter. Included with the counter is a read back 32-bit latch and a 32-bit alarm function implemented with a 32-bit comparator. The functions are described in **Clock and Alarm Data Registers**. The alarm has dual functions depending on whether the device is operational or in a power-down mode.

During operational mode, the alarm functions as a normal alarm comparing the current value of the 32-bit counter with the value written into the alarm latch bytes ($24–$27). Interrupts may be generated when a match occurs and when AE is set.

During the power-down mode, a successful compare can be used to drive the PSE pin high. When the Auto Restart bit (Control Register ($30), bit 5) is clear (i.e., zero), the PSE pin is driven high for 4 seconds. If V_{DD} is recognized to be greater than $V_{BAT} \times 1.25$ volts during the interval the PSE pin remains high. If the AR bit is set, then the PSE will be toggled using multiple attempts as described in **Auto-Restart Counters**.

10.0 RANDOM ACCESS MEMORY

The random access memory (RAM) is 64 × 8 bits, memory mapped from $00 to $1F (32 bytes) and from $40 to $5F (32 bytes). At Power-On Reset the value contained in the memory will be all ones ($FF). Address locations $60–$7F are reserved. The RAM is powered by the internal power bus.

11.0 TEST MODE

Test mode is entered when the TEST pin is taken to a high value. When the TEST pin is high, registers at locations $3E and $3F and $40–$4F are accessible. These registers are used for various test mode features and functions.

12.0 TEST REGISTERS

12.1 Test Register 1

BIT	7	6	5	4	3	2	1	0	
$3E Read	DIV1	VOVR	VDDUP	VDDON	VRT	0	0	0	TEST REGISTER 1
$3E Write	DIV1	VOVR	VDDUP	VDDON	LOW BAT	0	0	0	TEST REGISTER 1

Bit	Function
7	DIV1 — DIVIDE BY 1 When set, this bit enables the output of the 32-kHz oscillator to be connected to the NUC pin. This output can be monitored for correct frequency while the oscillator is tuned via the tuning bits in Test Register 2.
6	VOVR — V_{DD} OVERRIDE This bit is used to defeat the write protection ($V_{DD} < V_{BAT} \times 1.25$ V) feature. When VOVR is set to a 1 the part may be accessed at voltages below $V_{BAT} \times 1.25$ volts.
5	VDDUP — V_{DD} UP In a read cycle, this read/write bit, is used to determine whether the V_{DD} voltage is greater than $V_{BAT} \times 1.25$ volts. The bit is set to a 1 when $V_{DD} > V_{BAT} \times 1.25$ volts. When V_{DD} is below $V_{BAT} \times 1.25$ volts the RTC enters a write protect mode by disabling the chip enable pin. A read of this bit reports current status, While a write of this bit forces the VDDUP condition ($V_{DD} > V_{BAT} \times 1.25$) in a test condition, if the COMPOVR bit is set.

4 VDDON — V_{DD} ON
This read/write bit is used to determine whether V_{DD} voltage is greater than battery voltage (V_{BAT}). The bit is set to a 1 when $V_{DD} > V_{BAT}$. When VDDON is set to a 1 the internal power bus is powered by the V_{DD} pin. A read of this bit reports current status, While a write of this bit forces the VDDON condition ($V_{DD} > V_{BAT}$ in a test condition, if the COMPOVR bit is set.

3 VRT — VALID RAM AND TIME
In a read cycle, this read/write bit has a similar function as in the FTU bit in normal operational mode. It indicates that the battery voltage is greater than $V_{DD}/2.25$ volts. The bit is available in the test mode. VRT is cleared by a POR or $V_{BAT} > 2.2$ volts. A read of this bit reports current status, While a write of this bit forces the low battery condition ($V_{DD} > V_{BAT} \times 2.2$) in a test condition, if the COMPOVR bit is set.

2, 1, 0 PCC, PCB, PCA — PROGRAMMABLE CAPACITORS
These bits control whether three capacitors are added to the oscillator. They are used to trim the load capacitance of the crystal.
PCA — Smallest value capacitor (2.5 pF)
PCB — Medium value capacitor (5.0 pF)
PCC — Largest value capacitor (10.0 pF)

12.2 Test Register 2

BIT	7	6	5	4	3	2	1	0	
$3F	OSCBY	COMPOVR	POR	SELTCK	FRZ	DV2	DV1	DV0	TEST REGISTER 2

Bit **Function**

7 OSCBY — OSCILLATOR BYPASS
The internal oscillator bypass is used for testing. It bypasses the oscillator so that a higher speed clock may be used to simulate the 32.768 kHz crystal frequency.

6 COMPOVR — COMPARATOR OVERRIDE
When the TEST pin is high and when this bit is set, the CVDDUP, CVDDON, and CLOWBAT comparator outputs are overriden by TVDDUP, TVDDON, and TLOWBAT bits from TR1.

5 POR — POWER ON RESET
This bit is reserved for reporting status of any functions associated with the POR circuitry.

4 SELTCK — SELECT TEST CLOCK
When this bit is set, the 32-bit clock counter, the 15-bit oscillator divider, and the 18-bit auto-reset counter would receive incrementing clock from the writing of address $4F in these mode. This bit also segments the counters into byte sized sections (e.g., the 18-bit AR counter into section of 8-bits + 2-bits).

3 FRZ — FREEZE MODE
There are two modes to read the real time clock. 1) Freeze mode: where the 1 Hz clock edge that updates the counter is postponed if it collides with the serial interface read window, until the read operation is done. 2) Early-Read mode: A clock read is preformed at a time slot in the address cycle of the serial interface which is earlier than the actual read timing. A collision detection circuit monitors if the 1 Hz update clock edge collides with the early-read. If there is a collision, the regular read will be executed. Otherwise it is skipped. The POR default for this bit is the Early-Read mode.

2, 1, 0 DIV2, DIV1, DIV0 — DIVIDER BITS SELECT
These bits are used to bypass selected portions of the 15-bit divider chain. Zero, five, ten, or all stages of the divider chain may be bypassed. Additionally, the divider chain maybe reset using these bits (see Table 2). Similar functions for the 32-bit divider and the counters are also possible, but not currently implemented. At POR all the divider bits are reset to 0.

Table 2. Divider Select

DV2	DV1	DV0	Operation Mode	Divider Reset	Bypass First N-Divider Bits	Oscillator Mode
0	0	0	Test	No	0	On
0	0	1	Test	No	1 × (Note 1)	On
0	1	0	Test	No	0	Off
0	1	1	Test	No	5	On
1	0	0	Test	No	10	On
1	0	1	Test	No	All Stages	On
1	1	0	Test	Yes	0	On
1	1	1	Test	Yes	0	Off

NOTE 1: 32-kHz routed to NUC pin.

13.0 APPLICATION INFORMATION

Refer to Figure 6 for a typical PSE and $\overline{PSE}$ interface circuit.

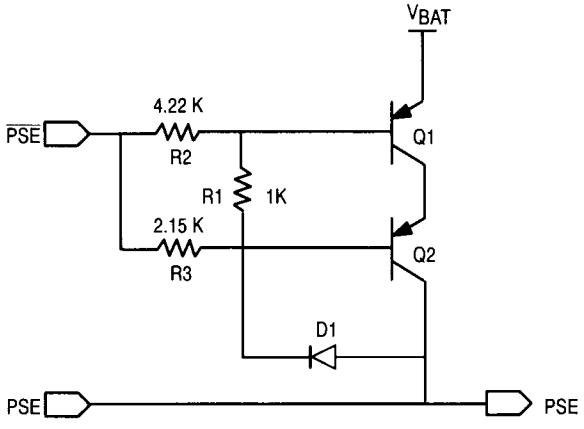
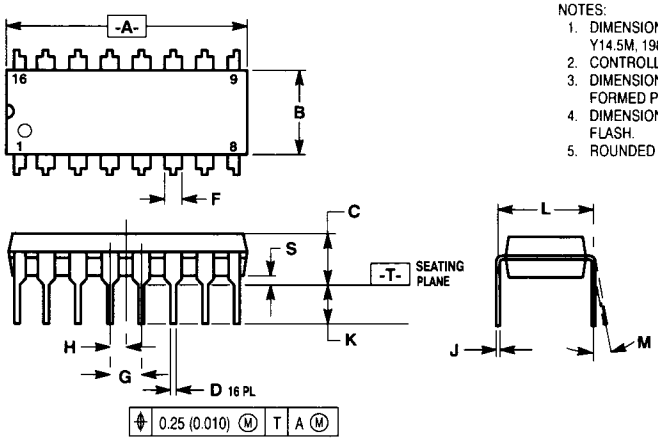


Figure 6. PSE and $\overline{PSE}$ Interface Circuit

14.0 PACKAGE DIMENSIONS

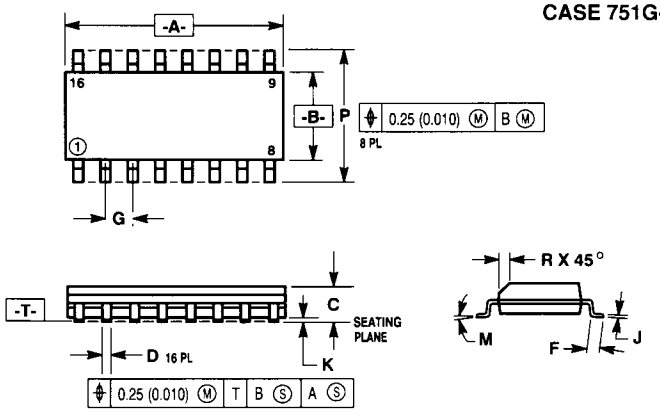
P SUFFIX
PLASTIC
CASE 648-08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

DW SUFFIX
SOG
CASE 751G-01



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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